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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,018	10/29/2003	Satoru Adachi	TIJ-35055	7078

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EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/696,018	ADACHI, SATORU	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-20* is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments to the claims filed 21 February 2007 have been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1 and 2** are rejected under 35 U.S.C. 102(b) as being anticipated by Dierickx (US 2002/0022309).

4. Regarding claim **1**, Dierickx discloses in Fig 7 a solid-state image sensing device comprising an integration of plural pixels (¶02), which has a light-receiving portion that receives light and generates and accumulates a signal charge (¶37), and has the following parts: a semiconductor substrate (6) of the first electroconductive type (n type); a semiconductor layer (3) of the second electroconductive type (p type) that is formed on the principal surface of said semiconductor substrate; a gate electrode for pixel selection (120) formed via a gate insulating film on said semiconductor layer; a first semiconductor region (1) of the first electroconductive type (n) that is formed in the outer layer (3) in the light-receiving portion positioned on one side of (120); a second semiconductor region (4) of the first electroconductive type formed deeper than said first region (1) in the outer layer of (43) in said light-receiving portion, wherein the

semiconductor substrate (5, p type), the semiconductor layer of the second electroconductive type (3, p type) and the second semiconductor region (4, n type) form a vertical transistor (vertical pnp transistor formed, see also ¶59); and a third semiconductor region (2) of the first electroconductive type (n) formed in the outer layer of (3) on the other side of the gate electrode (120) for pixel selection, and containing an impurity (n type) and having an impurity concentration higher than that of said first region (1) (item 2 is doped n++, compared to items 1 and 4, doped n).

5. With regards to claim **2**, Dierickx discloses in Figure 7 the device of claim 1, wherein the structure of the device is capable of performing the intended use limitations of the claim 2 language. That is, the device of claim 1 receives and accumulates charge in the semiconductor layer (3) of the light-receiving portion, and is capable of forming a junction transistor with the semiconductor substrate (6), semiconductor layer (1), and second semiconductor region (4), wherein the modulation of the threshold voltage of this junction transistor is performed by the signal charge accumulation in the semiconductor layer. If a prior art structure is capable of performing the intended use as recited in the preamble, then it meets the claim. See, e.g., In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

Allowable Subject Matter

6. Claims 3-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 7-20 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose or render obvious the device of claim 3, where a vertical transistor is formed by the substrate, second layer and second region, and wherein a gate electrode for reset and a fourth semiconductor region are formed, with said semiconductor layer, said reset gate, and said fourth region forming a buried-channel type of transistor. The prior art also does not disclose the device of claim 7, wherein a third semiconductor region of the second electroconductive type, having an impurity concentration higher than that of the first semiconductor region and formed on the semiconductor layer in the region facing said first region with said gate electrode for read sandwiched between them, said third semiconductor region and said substrate forming a vertical transistor.

Response to Arguments

9. Applicant's arguments filed 21 February 2007 have been fully considered but they are not persuasive. Regarding the argument that layer 3 of Dierickx is the same as substrate 6, these two similar layers form a vertical pnp transistor with n type region 4. Also, Dierickx discloses that an additional p type region may be formed in the n type region 4 to form a completely vertical transistor (¶59).

10. Applicant's arguments, see page 8 and 9, filed 21 February 2007, with respect to claims 3-20 have been fully considered and are persuasive. The rejection under 35 USC 103 of these claims has been withdrawn.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John C Ingham
Examiner
Art Unit 2814

jci

HOWARD WEISS
PRIMARY EXAMINER